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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/070,256	03/04/2002	Norihiko Sugita	TAMA 0002	2968

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EXAMINER	
IM, JUNGHWA M	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 12/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/070,256	SUGITA ET AL.	
	Examiner	Art Unit	
	Junghwa M. Im	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 September 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2 and 5-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 5-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *03/04/02, 09/22/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Goetz et al. (US 6175161), hereinafter Goetz in view of Yoshikawa (US 6199150).

Regarding claim 1, Fig. 5B of Goetz shows a multichip module including a module substrate (12) having including a module substrate having plural wiring layers (12a-12d in Fig. 4), a plurality of external connecting electrodes (15a, 15b in Fig. 4) formed on one face of said module substrate, and a plurality of mounting pads pad (21, 22 in Fig. 3) for mounting a plurality of semiconductor integrated circuit chips formed on the other face of said module substrate.

Fig. 5B of Goetz shows the most aspect of the instant invention except "wherein an area of said module substrate allocated to said plurality of mounting pad pads is separated into an area of the for a mounting pad of the semiconductor integrated circuit chips operated at relatively high speed, and an area of for a mounting pad of the semiconductor integrated circuit chips operated at relatively low speed, wherein external connecting electrodes of the plurality of external connecting electrodes for address outputs and data inputs-outputs are arranged on a rear face of said module substrate corresponding to said area for the mounting pad for semiconductor

integrated circuit chips operated at relatively low speed on a front face of said module substrate for mounting the semiconductor integrated circuit chips operated at relatively low speed, and

wherein said area for the mounting pad for semiconductor integrated circuit chips operated at relatively low speed on the front face of said module substrate is coupled to the external connecting electrodes of said plurality of external connecting electrodes for said address outputs and said data inputs-outputs operated at relatively low speed." Fig. 1 of Yoshikawa shows a configuration wherein a device mounting area is divided into regions for a high speed device and a low speed device and an address can be output to a low-speed device (col. 5, lines 7-13) while a data can be accessed and stored at low speed (col. 2, lines 27-33). Note that external connecting electrodes are needed to make a connection between the semiconductor device and the wiring substrate and this aspect is shown in Fig. 5B of Goetz.

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teachings of Yoshikawa into the device of Goetz in order to arrange the chips in high speeding and low speeding areas to improve the efficiency of the memory system.

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Goetz and Yoshikawa in view of Shenoy et al. (US 6198635), hereinafter Shenoy.

Regarding claim 2, the combined teachings of Goetz and Yoshikawa show the most aspect of the pending claim except "external connecting electrodes of the plurality of external connecting electrodes allocated to the supply of a power voltage and a ground voltage are arranged on the rear face of said module substrate corresponding to said area for the mounting pad for semiconductor integrated circuit chips operated at relatively high speed on the front face

of said module substrate for mounting the semiconductor integrated circuit chips operated at relatively high speed." Fig. 8 of Shenoy shows external connecting electrodes of the plurality of external connecting electrodes allocated to the supply of a power voltage and a ground voltage are arranged on all over the rear face of the semiconductor device.

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teaching of Shenoy into the device of Goetz and Yoshikawa in order to have the electrodes for power and ground allocated on the rear surface of the module substrate to operate the device.

Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Goetz in view of Smits (US 5432913) and Takemae et al. (US 6078514), hereafter Takemae.

Regarding claims 5 and 6, Fig. 5B of Goetz shows a multichip module including a module substrate (12) having plurality of wiring layers (12a-12d in Fig. 4), plurality of external connecting electrodes (15b, 17b in Fig. 4) formed on one face of said module substrate and semiconductor integrated circuit chips formed the other face of said module substrate.

Goetz fails to show that plural semiconductor integrated circuit chips are processor chip, memory chips and buffer circuits and wherein external connecting electrodes allocated to supply a power voltage and a ground voltage are arranged on the rear face of an area for mounting said memory chip for larger power consumption. Fig. 4A of Smits shows a module wherein the data processor chip (CPU), the plural memory chips (SRAM) and the plural buffer circuits are arranged.

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teachings of Smits into the device of Smits in order to have the recited arrangement of the chips to increase the efficiency of the date transfer.

The combined teachings of Goetz and Smits show the most aspect of the instant invention except "external connecting electrodes of the plurality of external connecting electrodes allocated to supply a power voltage and a ground voltage are arranged on the rear face of an area for mounting the memory chip. Fig. 5 of Takemae shows power supply pads (23) for power and ground in the high speed circuits (21; having lager power consumption).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teachings of Takemae into the device of Goetz and Smits in order to arrange the external connecting electrodes (connected to the corresponding pads) for the power supply to improve the data transfer speed.

Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Goetz in view of Smits.

Regarding claim 7, Fig. 5B of Goetz shows a multichip module including

a module substrate (12) having plurality of wiring layers (12a-12d in Fig. 4), plurality of external connecting electrodes (15b, 17b in Fig. 4) formed on one face of said module substrate and plurality of semiconductor integrated circuit chips formed the other face of said module substrate, and

wherein the mounting pattern and said plurality of external connecting electrodes are electroconductively coupled to each other through a corresponding anisotropic electroconductive film (through the wiring layer).

Fig. 5B of Goetz fails to show that the same kind of the devices are arranged in a region of the mounting area. Fig. 1 of Smits shows a module comprising a CPU, memories and buffers while the same kind of the devices are arranged in a region of the mounting area.

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teachings of Smits into the device of Goetz in order to have the same kind of the device grouped in one region of the mounting area for compact packaging.

Note that "anisotropic" is a process designation and would thus not carry patentable weight in this claim drawn to a product. See *In re Thorp,* 227 USPQ 964 (Fed. Cir. 1985).

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Goetz in view of Sato (US 5729764).

Regarding claim 8, Fig. 5B of Goetz shows a multichip module including a module substrate (12) having plurality of wiring layers (12a-12d in Fig. 4), plurality of external connecting electrodes (15b, 17b in Fig. 4) formed on one face of said module substrate and plurality of semiconductor integrated circuit chips (21, 22) formed the other face of said module substrate.

Goetz fails to show two semiconductor devices operating at different speeds and a functionality of the buffer circuit. Fig. 1 of Sato shows an integrated circuit device comprising a CPU, a memory circuit and a buffer circuit and the buffer circuit controls(interrupts) input data

through a CPU (col. 2, lines 36-64).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teachings of Sato into the device of Goetz in order to form a circuit recited in the instant invention for a desired circuit configuration.

Note that it would be obvious for the memory chip and the CPU operate at higher speed than the buffer circuit since the buffer circuit disables the data outputting (col. 2, lines 53-64).

And as discussed above, it is obvious to have the external connection electrodes for an address and data for the buffer circuit arranged on the rear mounting surface of the buffer device.

Response to Arguments

Applicant's arguments with respect to pending claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Junghwa M. Im whose telephone number is (571) 272-1655. The examiner can normally be reached on MON.-FRI. 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

jmi

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